IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

VLSI TECHNOLOGY LLC, *Plaintiff*	§	
	§	**A-19-CV-00977-ADA**
-vs-	§	
INTEL CORPORATION, *Defendant*	§	

CLAIM CONSTRUCTION ORDER

Before the Court are the Parties' claim construction briefs. ECF Nos. 81 (VLSI Tech opening), 82 (Intel opening), 84 (Intel response), 85 (VLSI Tech response), 89 (Intel reply), and 90 (VLSI Tech reply). The Court held the claim construction hearing on December 12, 2019. During that hearing, the Court provided complete constructions for all disputed terms except for "capacitance structure." This order provides the Court's constructions for all terms, and does not alter any of the constructions the Court provided at the hearing.

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I. U.S. PATENT NO. 6,366,522

Claim Term	Claim Construction
"regulate/regulating at least one supply from a power source and an inductance"	Plain and ordinary meaning (Transcript at 50:22-51:2)

II. U.S. PATENT NO. 7,292,485

Claim Term	Claim Construction
"a capacitance structure"	"a structure that is capable of storing and discharging electrical charge"
"precharging means for precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells"	**Function**: "precharging the capacitance structure to a predetermined voltage prior to a write operation for the second line of memory cells"

	Structure: "(1) Voltage source V_{REF} coupled in series with conductor 37, as shown in Figure 2, and equivalents thereof or (2) voltage source V_{REF} coupled in series with conductor 71, as shown in Figure 3, and equivalents thereof" (Transcript at 89:3-9)
"first coupling means for coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells"	**Function**: "coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells" **Structure**: "Transistor 52 or transistor 96, and equivalents thereof" (Transcript at 115:23-116:5, 116:24-117:3)
"second coupling means for coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells"	**Function**: "coupling the second supply line to the first capacitance structure during the write operation for the second line of memory cells" **Structure**: "Transistor 54 or transistor 94, and equivalents thereof" (Transcript at 116:6-12, 116:24-117:3)
"decoupling means for decoupling the first power supply line from the second line of memory cells during the write operation for the second line of memory cells"	Indefinite (Transcript at 127:24-128:6)

III. U.S. PATENT NO. 7,523,373

Claim Term	Claim Construction
"means for providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage"	**Function**: "providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage" **Structure**: "Power supply selector, and equivalents thereof" (Transcript at 158:13-19)

IV. U.S. PATENT NO. 7,606,983

Claim Term	Claim Construction
"an indication of a/the specified order"	Plain and ordinary meaning (Transcript at 185:4-6)

V. U.S. PATENT NO. 7,793,025

Claim Term	Claim Construction
"priority level information associated with a [first/second] system mode for each of the one or more interrupt requests" / "priority level information associated with a [first/second] system mode"	Plain and ordinary meaning (Transcript at 208:15-16)
"storage device for storing priority level information" / "sets of priority levels in … storage devices"	Plain and ordinary meaning (Transcript at 223:25-224:1)
"providing a plurality of interrupt priority storage devices comprising a first interrupt priority storage device for storing priority level information associated with a first system mode, and a second interrupt priority storage device for storing priority level information associated with a second system mode; and providing a plurality of interrupt priority storage devices comprising a first interrupt priority storage device for storing priority level information associated with a first system mode for each of the one or more interrupt requests, and a second interrupt priority storage device for storing priority level information associated with a second system mode for each of the one or more interrupt requests"	Not indefinite (Transcript at 239:17-23)

SIGNED this 3rd day of January, 2020.

ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE